

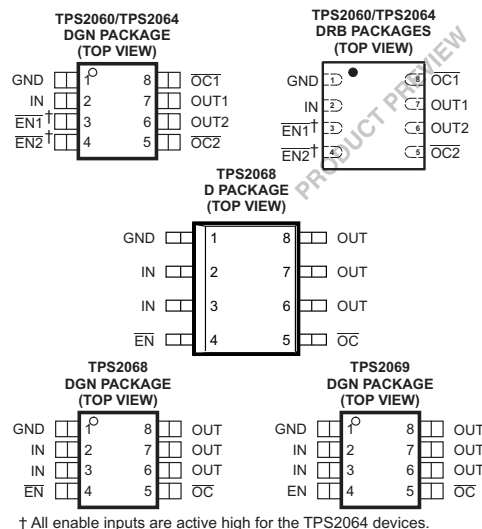
## CURRENT-LIMITED, POWER-DISTRIBUTION SWITCHES

### FEATURES

- 70-mΩ High-Side MOSFET
- 1.5-A Continuous Current
- Thermal and Short-Circuit Protection
- Accurate Current Limit (1.6 A min, 2.6 A max)
- Operating Range: 2.7 V to 5.5 V
- 0.6-ms Typical Rise Time
- Undervoltage Lockout
- Deglitched Fault Report ( $\overline{OC}$ )
- No  $\overline{OC}$  Glitch During Power Up
- 1-μA Maximum Standby Supply Current
- Reverse Current Blocking
- TPS2060/64 Temperature Range: 0°C to 70°C
- TPS2068/69 DGN Package Temperature Range: -40°C to 85°C
- TPS2068 D Package Temperature Range: 0°C to 70°C
- UL Listed – File No. E169910

### APPLICATIONS

- Heavy Capacitive Loads
- Short-Circuit Protections



### DESCRIPTION

The TPS206x power-distribution switches are intended for applications where heavy capacitive loads and short-circuits are likely to be encountered. This device incorporates 70-mΩ N-channel MOSFET power switches for power-distribution systems that require single or dual power switches in a single package. Each switch is controlled by a logic enable input. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the device limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ( $\overline{OCx}$ ) logic output low. When continuous heavy overloads and short-circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures that the switch remains off until valid input voltage is present. Current limit is typically 2.1 A.

GENERAL SWITCH CATALOG						
33 mΩ, Single  TPS201xA 0.2 A to 2 A TPS202x 0.2 A to 2 A TPS203x 0.2 A to 2 A	80 mΩ, Single  TPS2014 600 mA TPS2015 1 A TPS2041B 500 mA TPS2051B 500 mA TPS2045A 250 mA TPS2049 100 mA TPS2055A 250 mA TPS2061 1 A TPS2065 1 A TPS2068 1.5 A TPS2069 1.5 A	80 mΩ, Dual  TPS2042B 500 mA TPS2052B 500 mA TPS2046B 250 mA TPS2056 250 mA TPS2062 1 A TPS2066 1 A TPS2060 1.5 A TPS2064 1.5 A	80 mΩ, Dual  TPS2080 500 mA TPS2081 500 mA TPS2082 500 mA TPS2090 250 mA TPS2091 250 mA TPS2092 250 mA	80 mΩ, Triple  TPS2043B 500 mA TPS2053B 500 mA TPS2047B 250 mA TPS2057A 250 mA TPS2063 1 A TPS2067 1 A	80 mΩ, Quad  TPS2044B 500 mA TPS2054B 500 mA TPS2048A 250 mA TPS2058 250 mA	80 mΩ, Quad  TPS2085 500 mA TPS2086 500 mA TPS2087 500 mA TPS2095 250 mA TPS2096 250 mA TPS2097 250 mA



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### AVAILABLE OPTION AND ORDERING INFORMATION

T <sub>A</sub>	ENABLE	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C	NUMBER OF SWITCHES	PACKAGED DEVICES <sup>(1)(2)</sup>	
					MSOP (DGN)	SON (DRB)
0°C to 70°C	Active low	1.5 A	2.1 A	Dual	TPS2060DGN	TPS2060DRB <sup>(3)</sup>
	Active high				TPS2064DGN	TPS2064DRB <sup>(3)</sup>
-40°C to 85°C	Active low			Single	TPS2068DGN	
	Active high				TPS2069DGN	
0°C to 70°C	Active low			Single	TPS2068D	

(1) The package is available taped and reeled. Add an R suffix to device types (e.g., TPS2060DGN).

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

(3) Product Preview

### ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted <sup>(1)</sup>

		UNIT	
V <sub>I</sub>	Input voltage range, V <sub>I(IN)</sub>	-0.3 V to 6 V	
	Input voltage range, V <sub>I(ENx)</sub> , V <sub>I(ENx)</sub>	-0.3 V to 6 V	
	Voltage range, V <sub>I(OC)</sub> , V <sub>I(OCx)</sub>	-0.3 V to 6 V	
V <sub>O</sub>	Output voltage range, V <sub>O(OUT)</sub> , V <sub>O(OUTx)</sub>	-0.3 V to 6 V	
I <sub>O</sub>	Continuous output current, I <sub>O(OUT)</sub> , I <sub>O(OUTx)</sub>	Internally limited	
Continuous total power dissipation		See Dissipation Rating Table	
T <sub>J</sub>	Operating virtual junction temperature range	TPS2060/64	0°C to 105°C
		TPS2068/69 (DGN Package)	-40°C to 105°C
		TPS2068 (D Package)	0°C to 105°C
T <sub>stg</sub>	Storage temperature range	-65°C to 150°C	
ESD	Electrostatic discharge protection	Human body model MIL-STD-883C	2 kV
		Charge device model (CDM)	500 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### DISSIPATING RATING TABLE <sup>(1)</sup>

PACKAGE	THERMAL RESISTANCE θ <sub>JA</sub>	T <sub>A</sub> < 25°C POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING
DGN-8		1370 mW	17 mW/°C	600 mW	342 mW
D-8		585.82 mW	5.8582 mW/°C	322.20 mW	234.32 mW
DRB-8 (Low-K) <sup>(2)</sup>	270 °C/W	370 mW	3.71 mW/°C	203 mW	148 mW
DRB-8 (High-K) <sup>(3)</sup>	60 °C/W	1600 mW	16.67 mW/°C	916 mW	866 mW

(1) Heatsink the PowerPad™ per the recommendations of [SLMA002A](#). PCB used for recommendations per appendix A4.

(2) Soldered PowerPAD on a standard 2-layer PCB without vias for thermal pad. See TI application note [SLMA002](#) for further details.

(3) Soldered PowerPAD on a standard 4-layer PCB with vias for thermal pad. See TI application note [SLMA002](#) for further details.

## RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT	
V <sub>I</sub>	Input voltage, V <sub>I(IN)</sub>	2.7	5.5	V	
	Input voltage, V <sub>I(ENX)</sub> , V <sub>I(ENX)</sub>	0	5.5	V	
I <sub>O</sub>	Continuous output current, I <sub>O(OUTX)</sub>	0	1.5	A	
T <sub>J</sub>	Operating virtual junction temperature	TPS2060/64	0	105	°C
		TPS2068/69 (DGN Package)	–40	105	
		TPS2068 (D Package)	0	105	

## ELECTRICAL CHARACTERISTICS

0°C ≤ T<sub>J</sub> ≤ 105°C for the TPS2060/64 and TPS2068 (D package), plus –40°C ≤ T<sub>J</sub> ≤ 105° for the TPS2068/69 (DGN package), V<sub>I(IN)</sub> = 5.5 V, I<sub>O</sub> = 1 A, V<sub>I(ENX)</sub> = 0 V, or V<sub>I(ENX)</sub> = 5.5 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS <sup>(1)</sup>		MIN	TYP	MAX	UNIT
<b>POWER SWITCH</b>							
r <sub>DS(on)</sub>	Static drain-source on-state resistance, 5-V operation and 3.3-V operation	V <sub>I(IN)</sub> = 5 V or 3.3 V, I <sub>O</sub> = 1.5 A		70	115		mΩ
	Static drain-source on-state resistance, 2.7-V operation	V <sub>I(IN)</sub> = 2.7 V, I <sub>O</sub> = 1.5 A		75	125		mΩ
t <sub>r</sub>	Rise time, output	V <sub>I(IN)</sub> = 5.5 V	C <sub>L</sub> = 1 μF, R <sub>L</sub> = 5 Ω	T <sub>J</sub> = 25°C	0.6	1.5	ms
		V <sub>I(IN)</sub> = 2.7 V			0.4	1	
t <sub>f</sub>	Fall time, output	V <sub>I(IN)</sub> = 5.5 V			0.05	0.5	
		V <sub>I(IN)</sub> = 2.7 V			0.05	0.5	
<b>ENABLE INPUT <math>\overline{\text{EN}}</math> OR EN</b>							
V <sub>IH</sub>	High-level input voltage	2.7 V < V <sub>I(IN)</sub> < 5.5 V		2			V
V <sub>IL</sub>	Low-level input voltage	2.7 V < V <sub>I(IN)</sub> < 5.5 V				0.8	
I <sub>I</sub>	Input current	V <sub>I(ENX)</sub> = 0 V or 5.5 V, V <sub>I(ENX)</sub> = 0 V or 5.5 V		–0.5		0.5	μA
t <sub>on</sub>	Turnon time	C <sub>L</sub> = 100 μF, R <sub>L</sub> = 5 Ω				3	ms
t <sub>off</sub>	Turnoff time	C <sub>L</sub> = 100 μF, R <sub>L</sub> = 5 Ω				10	
<b>CURRENT LIMIT</b>							
I <sub>OS</sub>	Short-circuit output current	V <sub>I(IN)</sub> = 5 V, OUT connected to GND, device enabled into short-circuit		1.6	2.1	2.6	A
I <sub>OC_TRIP</sub>	Overcurrent trip threshold	V <sub>I(IN)</sub> = 5 V, Current ramp (≤ 100 A/s) on OUT		TPS2060/64	3.2	3.9	A
				TPS2068/69	2.3	2.85	
I <sub>OS</sub> <sup>(2)</sup>	Short-circuit output current	V <sub>I(IN)</sub> = 5 V, OUT1 and OUT2 connected to GND, Device enabled into short-circuit, current measured at V <sub>I(IN)</sub>		3.2	4.2	5.2	A
I <sub>OC_TRIP</sub> <sup>(2)</sup>	Overcurrent trip threshold TPS2060/64	V <sub>I(IN)</sub> = 5 V, Current ramp (≤ 100 A/s) on OUT1 and OUT2 tied together, current measured at V <sub>I(IN)</sub>		6.4	7.8		A
I <sub>OL</sub>	Supply current, low-level output	No load on OUT, V <sub>I(ENX)</sub> = 5.5 V, or V <sub>I(ENX)</sub> = 0 V		T <sub>J</sub> = 25°C	0.5	1	μA
				Over T <sub>J</sub> range	0.5	5	
I <sub>OH</sub>	Supply current, high-level output TPS2060/64	No load on OUT, V <sub>I(ENX)</sub> = 0 V, or V <sub>I(ENX)</sub> = 5.5 V		T <sub>J</sub> = 25°C	50	70	μA
				Over T <sub>J</sub> range	50	90	
I <sub>OH</sub>	Supply current, high-level output TPS2068/69	No load on OUT, V <sub>I(ENX)</sub> = 0 V, or V <sub>I(ENX)</sub> = 5.5 V		T <sub>J</sub> = 25°C	43	60	μA
				Over T <sub>J</sub> range	43	70	
I <sub>lkg</sub>	Leakage current	OUT connected to ground, V <sub>I(ENX)</sub> = 5.5 V, or V <sub>I(ENX)</sub> = 0 V			1		μA
	Reverse leakage current	V <sub>I(OUTX)</sub> = 5.5 V, IN = ground		T <sub>J</sub> = 25°C	0.2		μA
<b>UNDERVOLTAGE LOCKOUT</b>							
	Low-level input voltage, IN			2		2.5	V
	Hysteresis, IN	T <sub>J</sub> = 25°C			75		mV

- (1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
- (2) This configuration has not been tested for UL certification.

**ELECTRICAL CHARACTERISTICS (continued)**

0°C ≤ T<sub>J</sub> ≤ 105°C for the TPS2060/64 and TPS2068 (D package), plus –40°C ≤ T<sub>J</sub> ≤ 105° for the TPS2068/69 (DGN package), V<sub>I(IN)</sub> = 5.5 V, I<sub>O</sub> = 1 A, V<sub>I(ENx)</sub> = 0 V, or V<sub>I(ENx)</sub> = 5.5 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS <sup>(1)</sup>	MIN	TYP	MAX	UNIT
<b>OVERCURRENT <math>\overline{OCx}</math></b>						
V <sub>OL(OCx)</sub>	Output low voltage	I <sub>O(OCx)</sub> = 5 mA			0.4	V
	Off-state current	V <sub>O(OCx)</sub> = 5 V or 3.3 V			1	μA
	$\overline{OC}$ deglitch	$\overline{OCx}$ assertion or deassertion	4	8	15	ms
<b>THERMAL SHUTDOWN<sup>(3)</sup></b>						
	Thermal shutdown threshold		135			°C
	Recovery from thermal shutdown		125			°C
	Hysteresis			10		°C

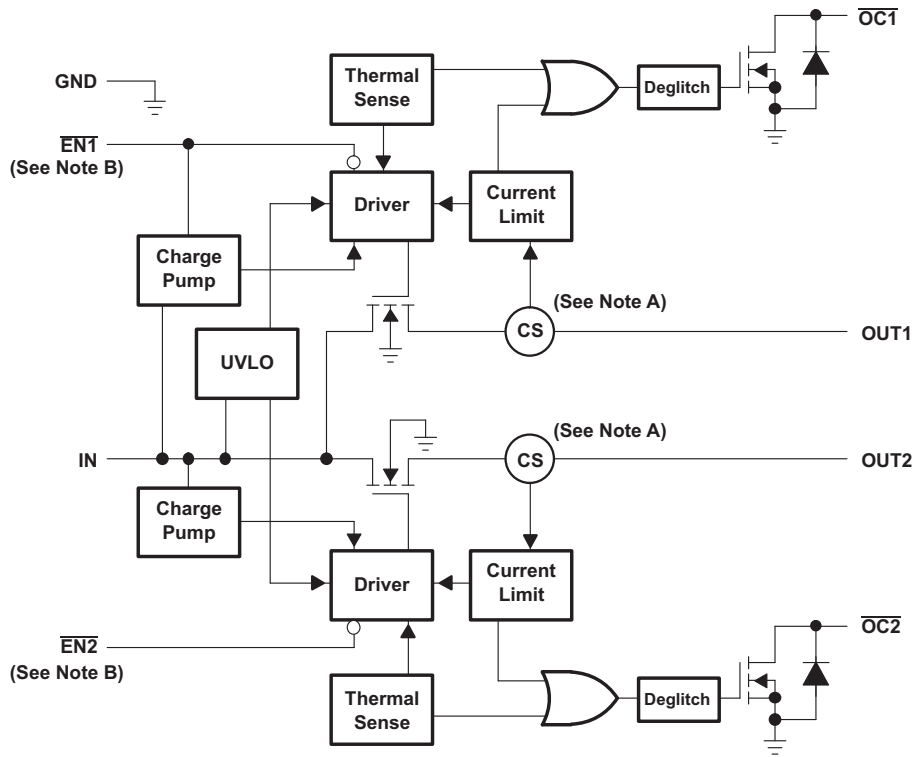
(3) The thermal shutdown only reacts under overcurrent conditions.

**DEVICE INFORMATION**

**Pin Functions**

PINS			I/O	DESCRIPTION
DGN and DRB PACKAGES				
NAME	TPS2060	TPS2064		
$\overline{EN1}$	3	—	I	Enable input, logic low turns on power switch IN-OUT1
$\overline{EN2}$	4	—	I	Enable input, logic low turns on power switch IN-OUT2
EN1	—	3	I	Enable input, logic high turns on power switch IN-OUT1
EN2	—	4	I	Enable input, logic high turns on power switch IN-OUT2
GND	1	1		Ground
IN	2	2	I	Input voltage
$\overline{OC1}$	8	8	O	Overcurrent, open-drain output, active low, IN-OUT1
$\overline{OC2}$	5	5	O	Overcurrent, open-drain output, active low, IN-OUT2
OUT1	7	7	O	Power-switch output, IN-OUT1
OUT2	6	6	O	Power-switch output, IN-OUT2
	PowerPad	PowerPad		Connect to GND

Functional Block Diagram (TPS2060 and TPS2064)



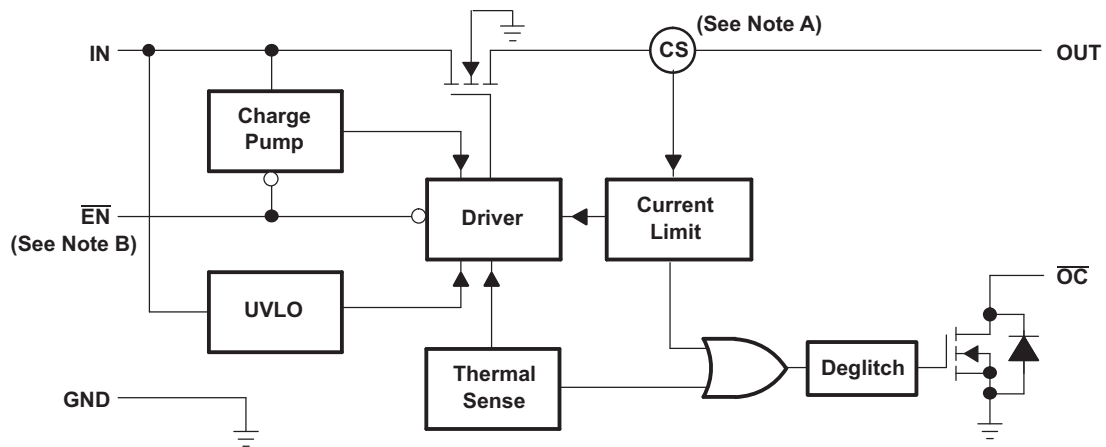
- A. Current sense.
- B. Active low ( $\overline{\text{ENx}}$ ) for TPS2060. Active high (ENx) for TPS2064.

## DEVICE INFORMATION

### Pin Functions (TPS2068 and TPS2069)

NAME	PINS		I/O	DESCRIPTION
	TPS2068	TPS2069		
$\overline{\text{EN}}$	4	—	I	Enable input, logic low turns on power switch
EN	—	4	I	Enable input, logic high turns on power switch
GND	1	1		Ground
IN	2, 3	2, 3	I	Input voltage
$\overline{\text{OC}}$	5	5	O	Overcurrent, open-drain output, active-low
OUT	6, 7, 8	6, 7, 8	O	Power-switch output
	PowerPad	PowerPad		Connect to GND (DGN Package Only)

### Functional Block Diagram (TPS2068 and TPS2069)



- A. Current sense.
- B. Active low ( $\overline{\text{EN}}$ ) for TPS2068. Active high (EN) for TPS2069.

PARAMETER MEASUREMENT INFORMATION

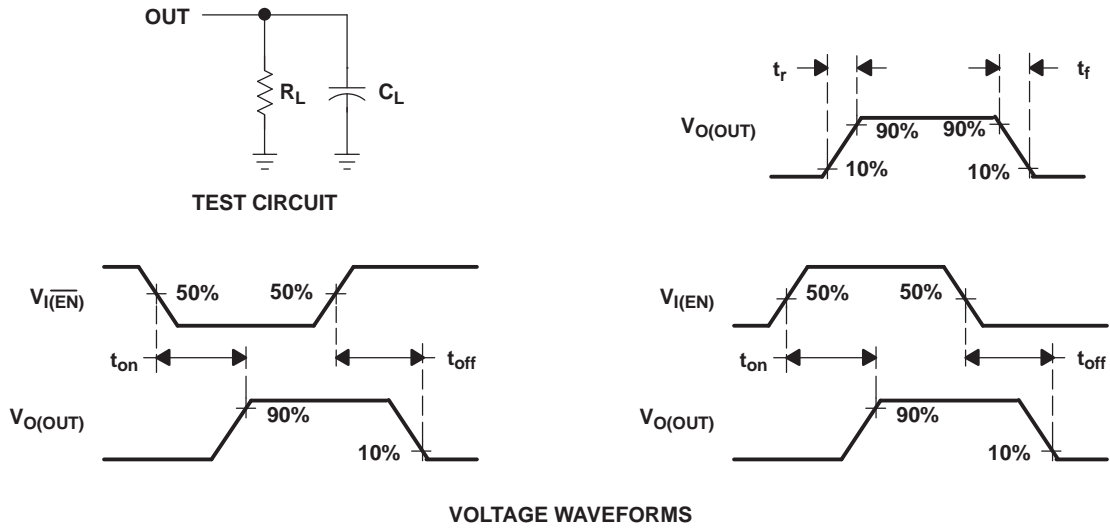


Figure 1. Test Circuit and Voltage Waveforms

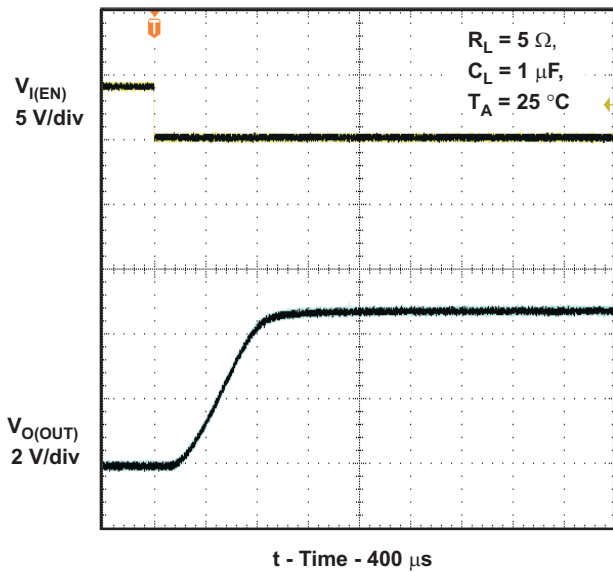


Figure 2. Turnon Delay and Rise Time With 1-μF Load

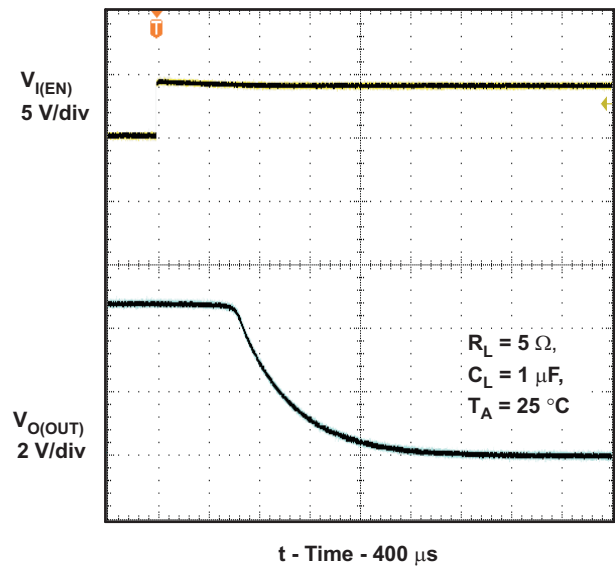
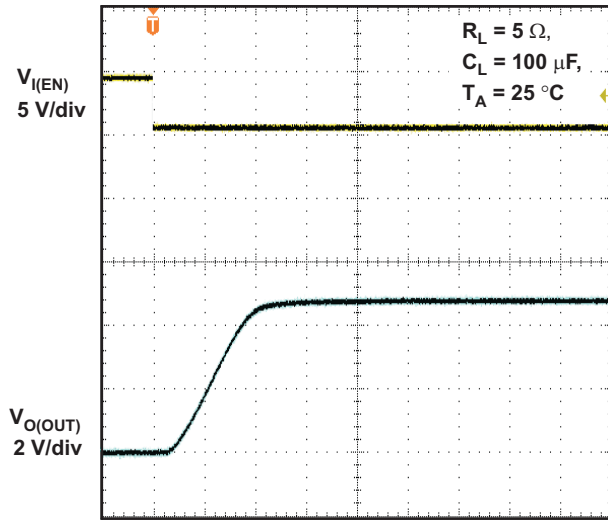


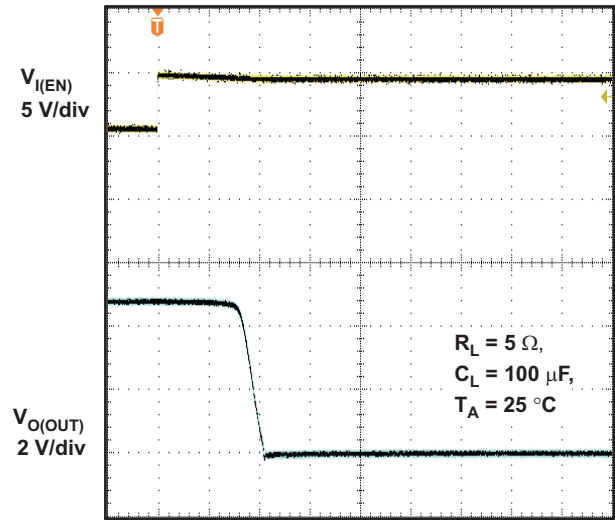
Figure 3. Turnoff Delay and Fall Time With 1-μF Load

PARAMETER MEASUREMENT INFORMATION (continued)



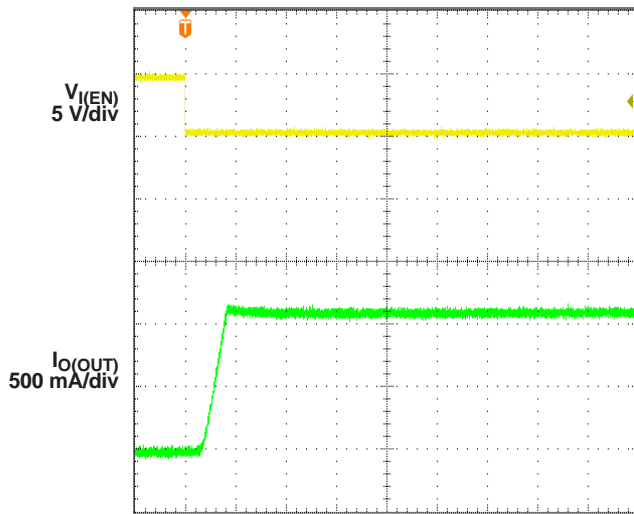
t - Time - 400  $\mu\text{s}$

Figure 4. Turnon Delay and Rise Time With 100- $\mu\text{F}$  Load



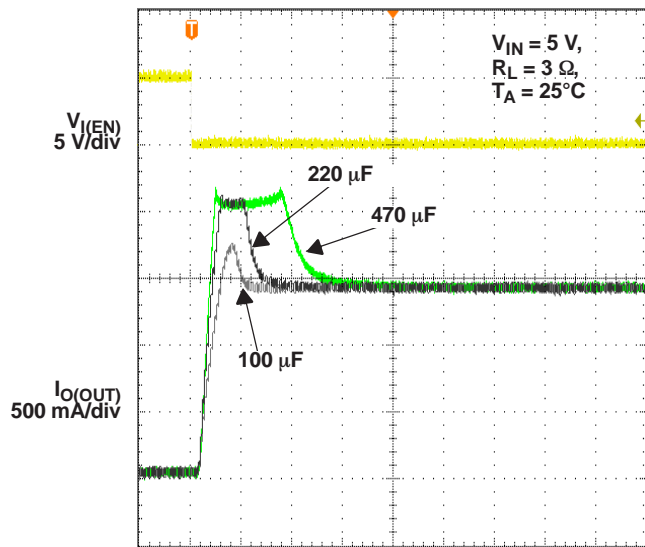
t - Time - 400  $\mu\text{s}$

Figure 5. Turnoff Delay and Fall Time With 100- $\mu\text{F}$  Load



t - Time - 500  $\mu\text{s/div}$

Figure 6. Short-Circuit Current, Device Enabled Into Short



t - Time - 500  $\mu\text{s/div}$

Figure 7. Inrush Current With Different Load Capacitance



PARAMETER MEASUREMENT INFORMATION (continued)

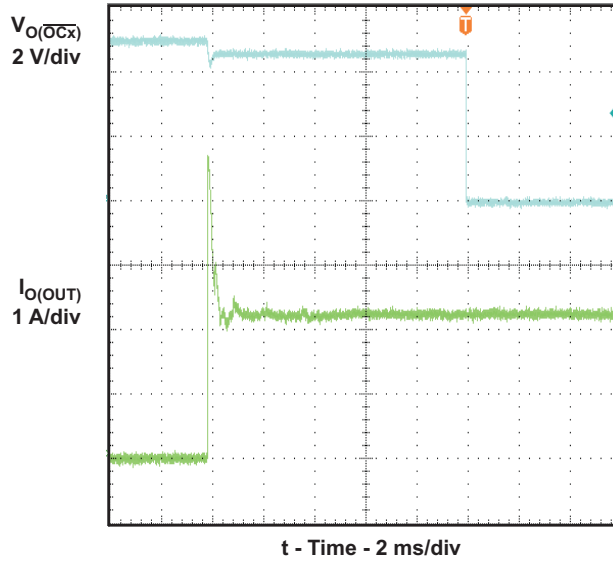


Figure 8. 0.6-Ω Load Connected to Enabled Device

TYPICAL CHARACTERISTICS

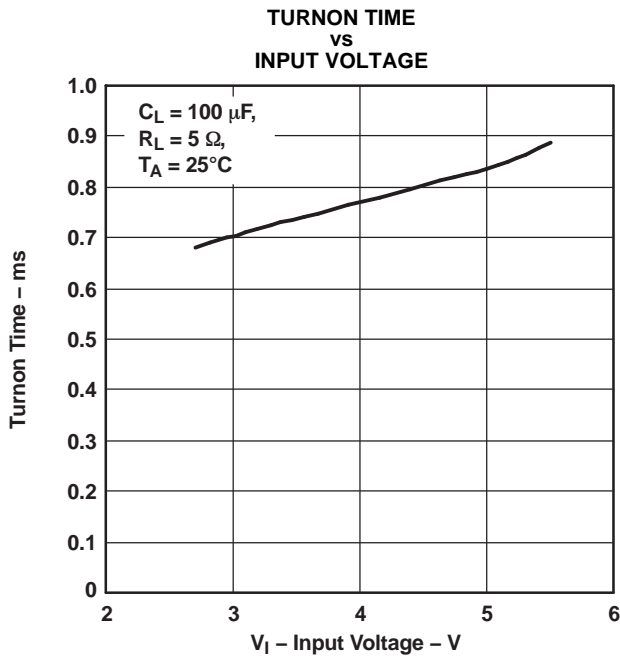


Figure 9.

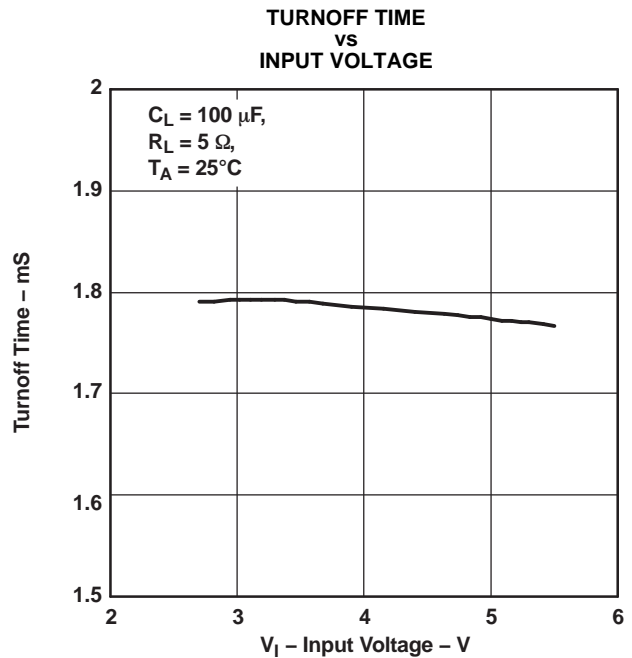


Figure 10.

TYPICAL CHARACTERISTICS (continued)

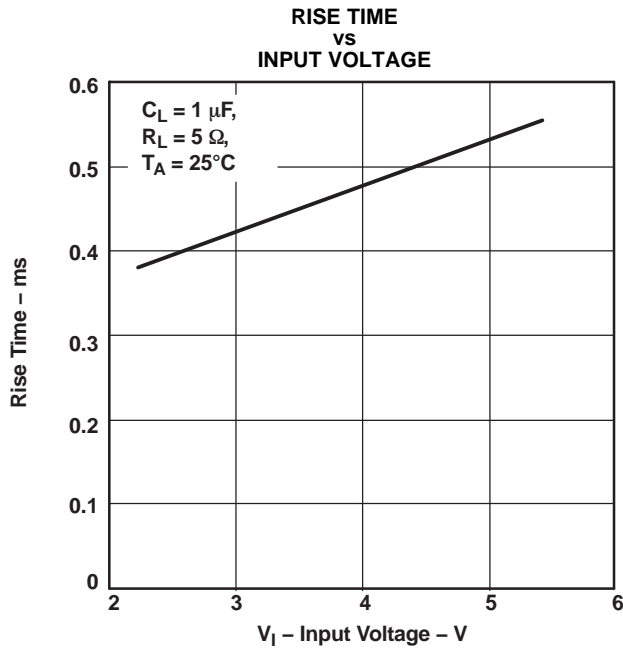


Figure 11.

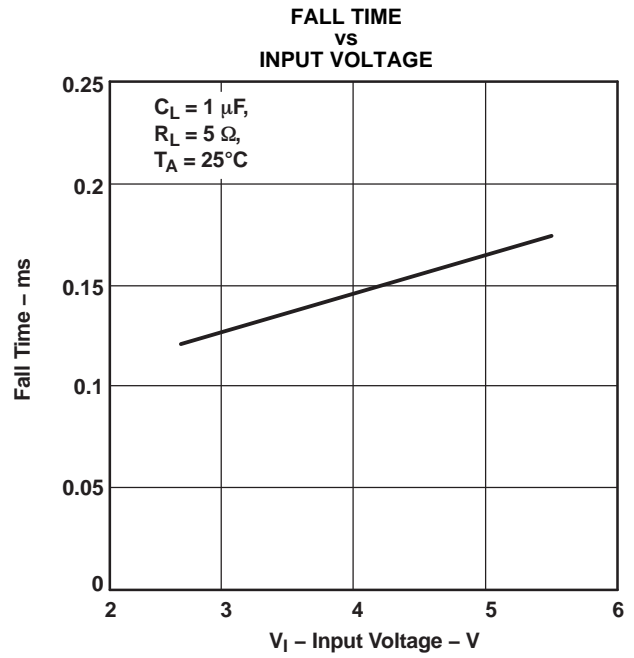


Figure 12.

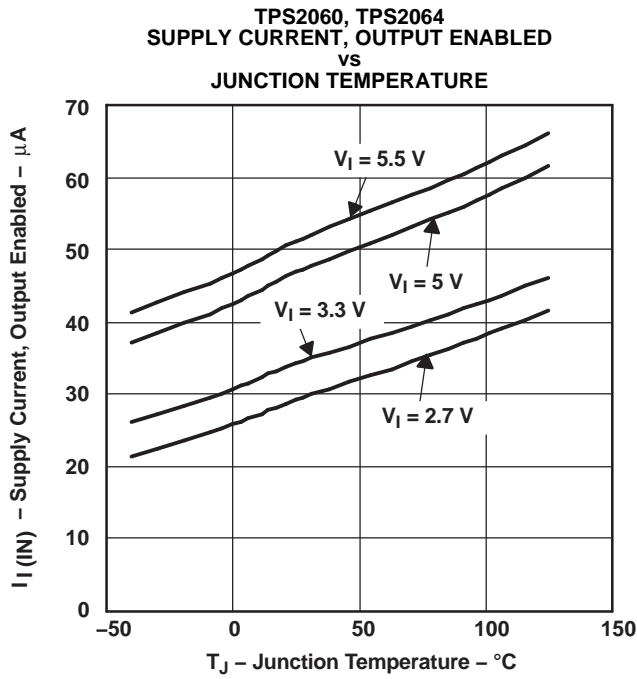


Figure 13.

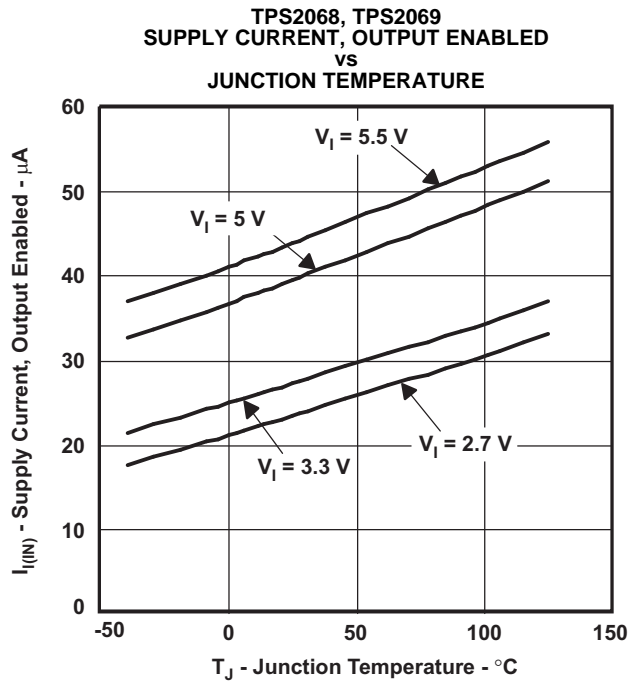


Figure 14.

TYPICAL CHARACTERISTICS (continued)

SUPPLY CURRENT, OUTPUT DISABLED  
vs  
JUNCTION TEMPERATURE

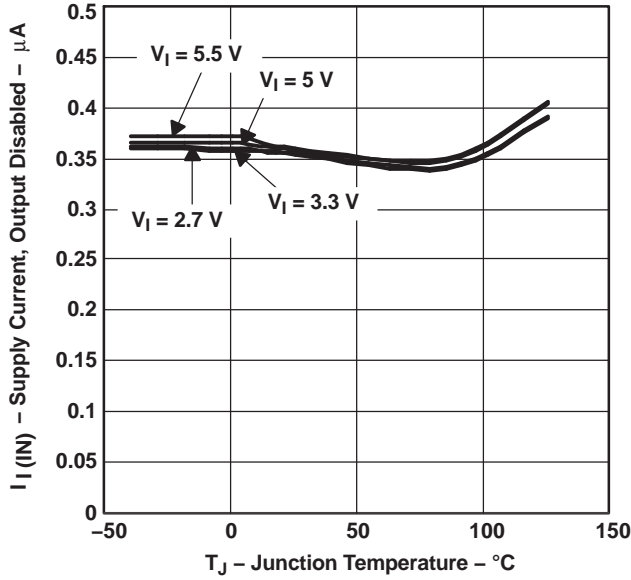


Figure 15.

STATIC DRAIN-SOURCE ON-STATE RESISTANCE  
vs  
JUNCTION TEMPERATURE

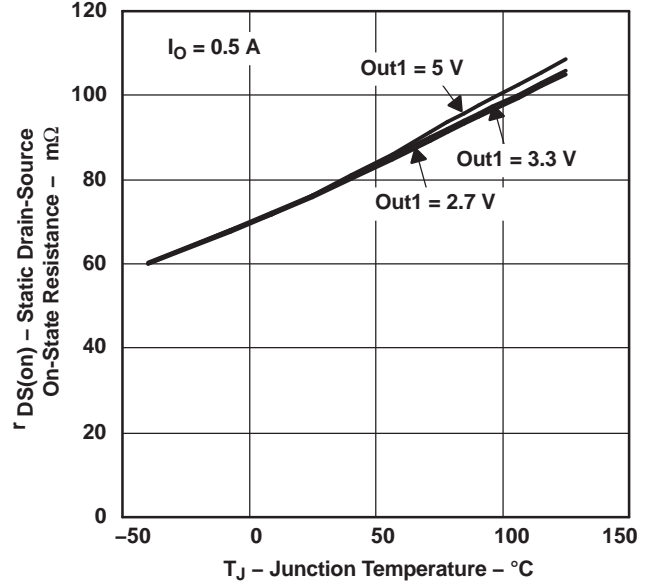


Figure 16.

SHORT-CIRCUIT OUTPUT CURRENT  
vs  
JUNCTION TEMPERATURE

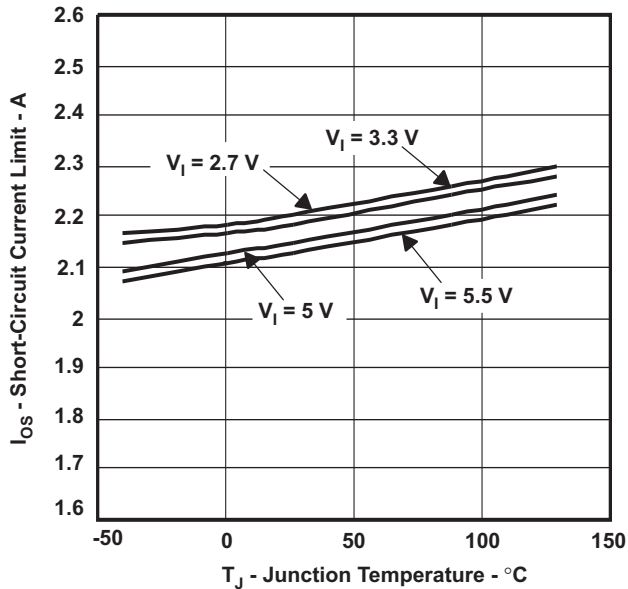


Figure 17.

UNDERVOLTAGE LOCKOUT  
vs  
JUNCTION TEMPERATURE

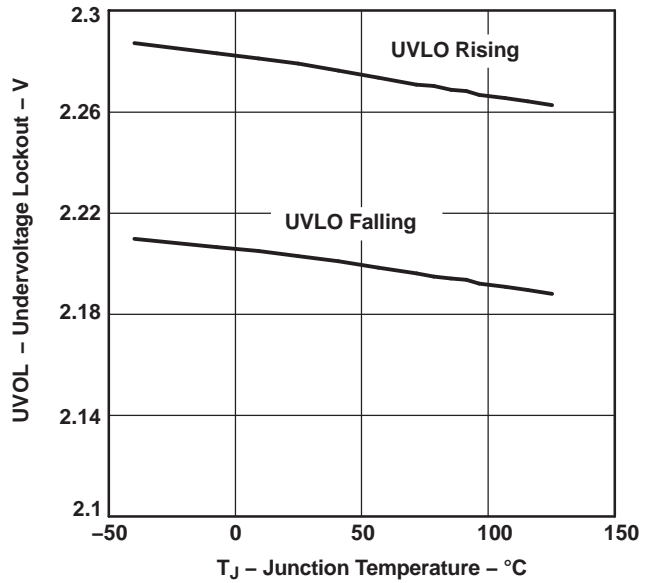
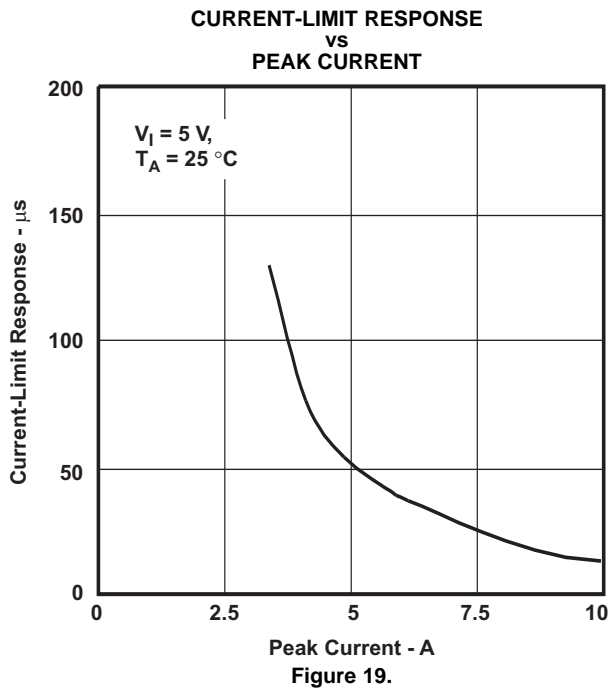


Figure 18.

### TYPICAL CHARACTERISTICS (continued)



## APPLICATION INFORMATION

### POWER-SUPPLY CONSIDERATIONS

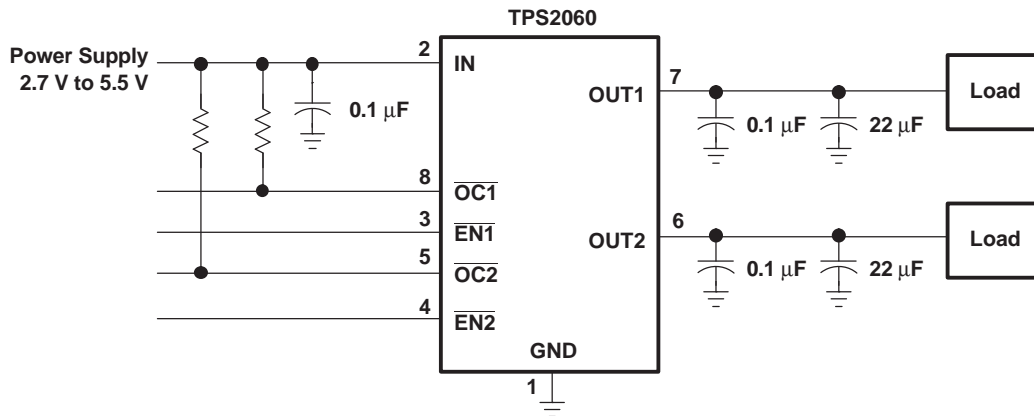


Figure 20. Typical Application

A 0.01- $\mu\text{F}$  to 0.1- $\mu\text{F}$  ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01- $\mu\text{F}$  to 0.1- $\mu\text{F}$  ceramic capacitor improves the immunity of the device to short-circuit transients.

### OVERCURRENT

A sense FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before  $V_{I(IN)}$  has been applied (see Figure 6). The TPS206x senses the short and immediately switches into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for a short period of time before the current-limit circuit can react (see Figure 8). After the current-limit circuit has tripped (reached the overcurrent trip threshold), the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded. The TPS206x is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

### OC RESPONSE

The  $\overline{\text{OCx}}$  open-drain output is asserted (active low) when an overcurrent or overtemperature shutdown condition is encountered after a 10-ms deglitch timeout. The output remains asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause a momentary overcurrent condition; however, no false reporting on  $\overline{\text{OCx}}$  occurs due to the 10-ms deglitch circuit. The TPS206x is designed to eliminate false overcurrent reporting. The internal overcurrent deglitch eliminates the need for external components to remove unwanted pulses.  $\overline{\text{OCx}}$  is not deglitched when the switch is turned off due to an overtemperature shutdown.

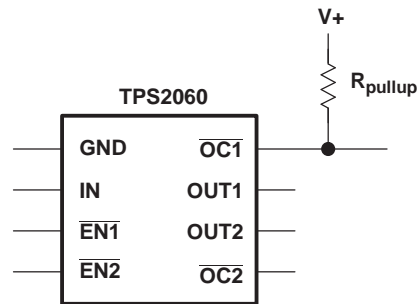


Figure 21. Typical Circuit for the  $\overline{OC}$  Pin

## POWER DISSIPATION AND JUNCTION TEMPERATURE

The low on-resistance on the N-channel MOSFET allows the small surface-mount packages to pass large currents. The thermal resistance of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. Begin by determining the  $r_{DS(on)}$  of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read  $r_{DS(on)}$  from [Figure 16](#). Using this value, the power dissipation per switch can be calculated by:

$$P_D = r_{DS(on)} \times I^2$$

Multiply this number by the number of switches being used. This step renders the total power dissipation from the N-channel MOSFETs.

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

$T_A$  = Ambient temperature °C

$R_{\theta JA}$  = Thermal resistance

$P_D$  = Total power dissipation based on number of switches being used.

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

## THERMAL PROTECTION

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The TPS206x implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. In an overcurrent or short-circuit condition, the junction temperature rises due to excessive power dissipation. Once the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 10°C, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The  $\overline{OCx}$  open-drain output is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

## UNDERVOLTAGE LOCKOUT (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch is quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO also keeps the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. On reinsertion, the power switch is turned on, with a controlled rise time to reduce EMI and voltage overshoots.

## UNIVERSAL SERIAL BUS (USB) APPLICATIONS

The universal serial bus (USB) interface is a 12-Mb/s, or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

SPHs and BPHs distribute data and power to downstream functions. The TPS206x has higher current capability than required by one USB port; so, it can be used on the host side and supplies power to multiple downstream ports or functions.

## HOST/SELF-POWERED AND BUS-POWERED HUBS

Hosts and SPHs have a local power supply that powers the embedded functions and the downstream ports (see [Figure 22](#)). This power supply must provide from 5.25 V to 4.75 V to the board side of the downstream connection under full-load and no-load conditions. Hosts and SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

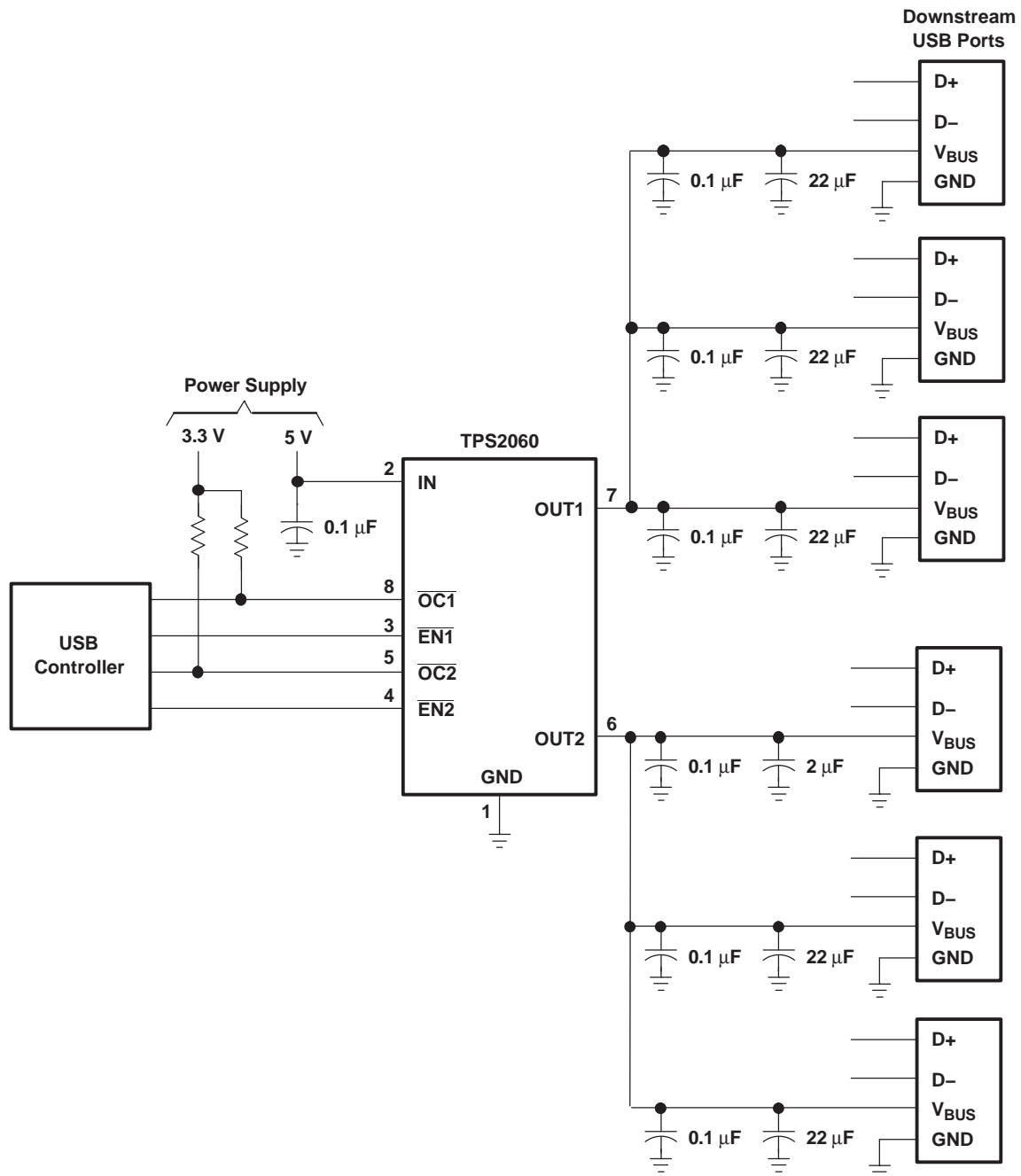


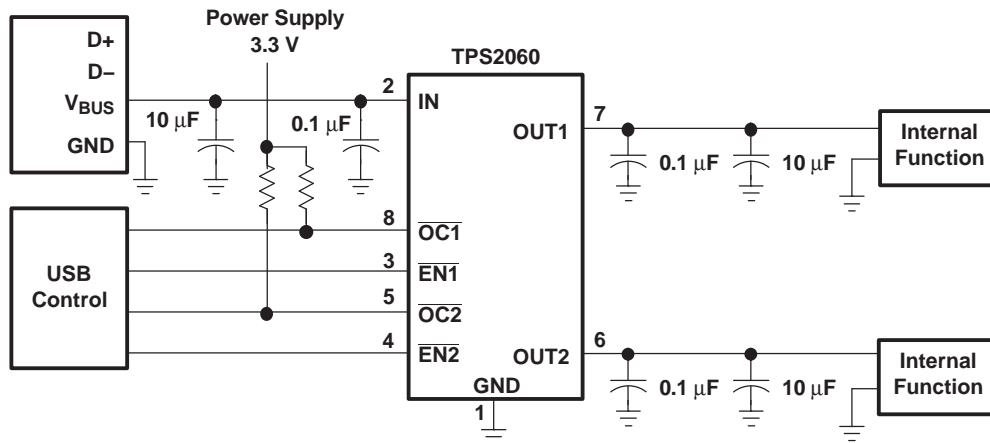
Figure 22. Typical Six-Port USB Host/Self-Powered Hub

BPHs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.



## LOW-POWER BUS-POWERED AND HIGH-POWER BUS-POWERED FUNCTIONS

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44  $\Omega$  and 10  $\mu\text{F}$  at power up, the device must implement inrush current limiting (see Figure 23). With TPS206x, the internal functions could draw more than 500 mA, which fits the needs of some applications such as motor driving circuits.



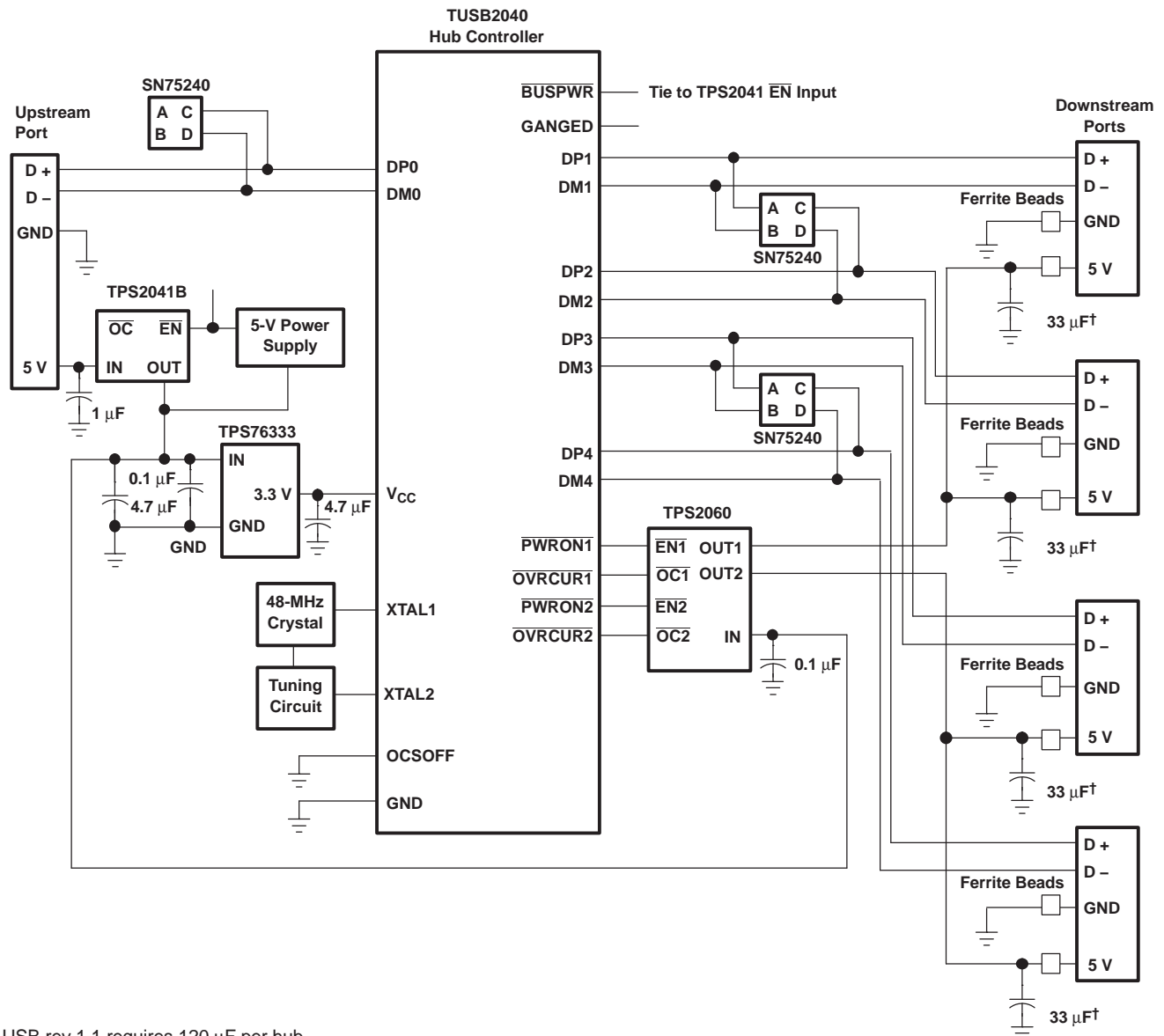
**Figure 23. High-Power Bus-Powered Function**

## USB POWER-DISTRIBUTION REQUIREMENTS

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power-distribution features must be implemented.

- Hosts/SPHs must:
  - Current-limit downstream ports
  - Report overcurrent conditions on USB  $V_{\text{BUS}}$
- BPHs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44  $\Omega$  and 10  $\mu\text{F}$ )
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

The feature set of the TPS206x allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-powered hubs, as well as the input ports for bus-powered functions (see Figure 24).



† USB rev 1.1 requires 120 µF per hub.

Figure 24. Hybrid Self / Bus-Powered Hub Implementation

## GENERIC HOT-PLUG APPLICATIONS

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS206x, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS206x also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion. The UVLO feature insures a soft start with a controlled rise time for every insertion of the card or module.

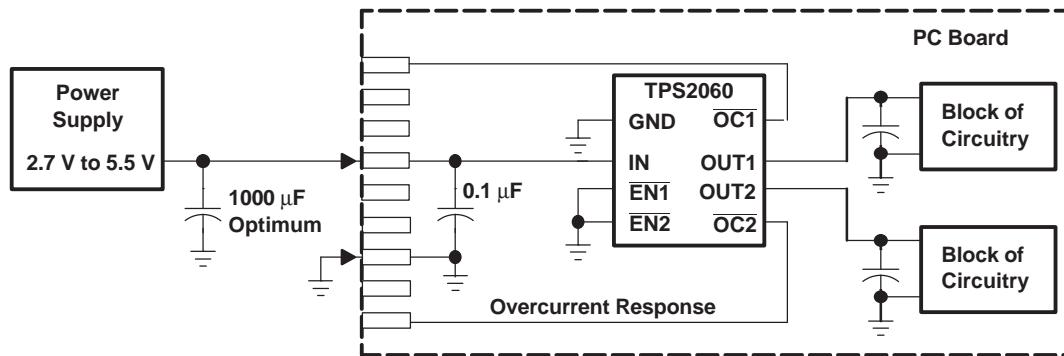


Figure 25. Typical Hot-Plug Implementation

By placing the TPS206x between the  $V_{CC}$  input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

## DETAILED DESCRIPTION

### Power Switch

The power switch is an N-channel MOSFET with a low on-state resistance. Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled. The power switch supplies a minimum current of 1.5 A.

### Charge Pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires little supply current.

### Driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage.

### Enable ( $\overline{ENx}$ )

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current. The supply current is reduced to less than 1  $\mu$ A when a logic high is present on  $\overline{ENx}$ , or when a logic low is present on  $\overline{ENx}$ . A logic zero input on  $\overline{ENx}$ , or a logic high input on  $\overline{ENx}$  restores bias to the drive and control circuits and turns the switch on. The enable input is compatible with both TTL and CMOS logic levels.

### Overcurrent ( $\overline{OCx}$ )

The  $\overline{OCx}$  open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output remains asserted until the overcurrent or overtemperature condition is removed. A 10-ms deglitch circuit prevents the  $\overline{OCx}$  signal from oscillation or false triggering. If an overtemperature shutdown occurs, the  $\overline{OCx}$  is asserted instantaneously.

## **Current Sense**

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load.

## **Thermal Sense**

The TPS206x implements a thermal sensing to monitor the operating temperature of the power distribution switch. In an overcurrent or short-circuit condition the junction temperature rises. When the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns off the switch, thus preventing the device from damage. Hysteresis is built into the thermal sense, and after the device has cooled approximately 10 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed. The open-drain false reporting output ( $\overline{OCx}$ ) is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

## **Undervoltage Lockout**

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPS2060DGN	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2060DGNG4	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2060DGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2060DGNRG4	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2060DRBR	PREVIEW	SON	DRB	8	3000	TBD	Call TI	Call TI
TPS2060DRBT	PREVIEW	SON	DRB	8	250	TBD	Call TI	Call TI
TPS2064DGN	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2064DGNG4	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2064DGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2064DGNRG4	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2064DRBR	PREVIEW	SON	DRB	8	3000	TBD	Call TI	Call TI
TPS2064DRBT	PREVIEW	SON	DRB	8	250	TBD	Call TI	Call TI
TPS2068D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS2068DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS2068DGN	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2068DGNG4	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2068DGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2068DGNRG4	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2068DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS2068DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS2069DGN	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPS2069DGNG4	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2069DGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2069DGNRG4	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2060DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS2064DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS2068DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS2068DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2069DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

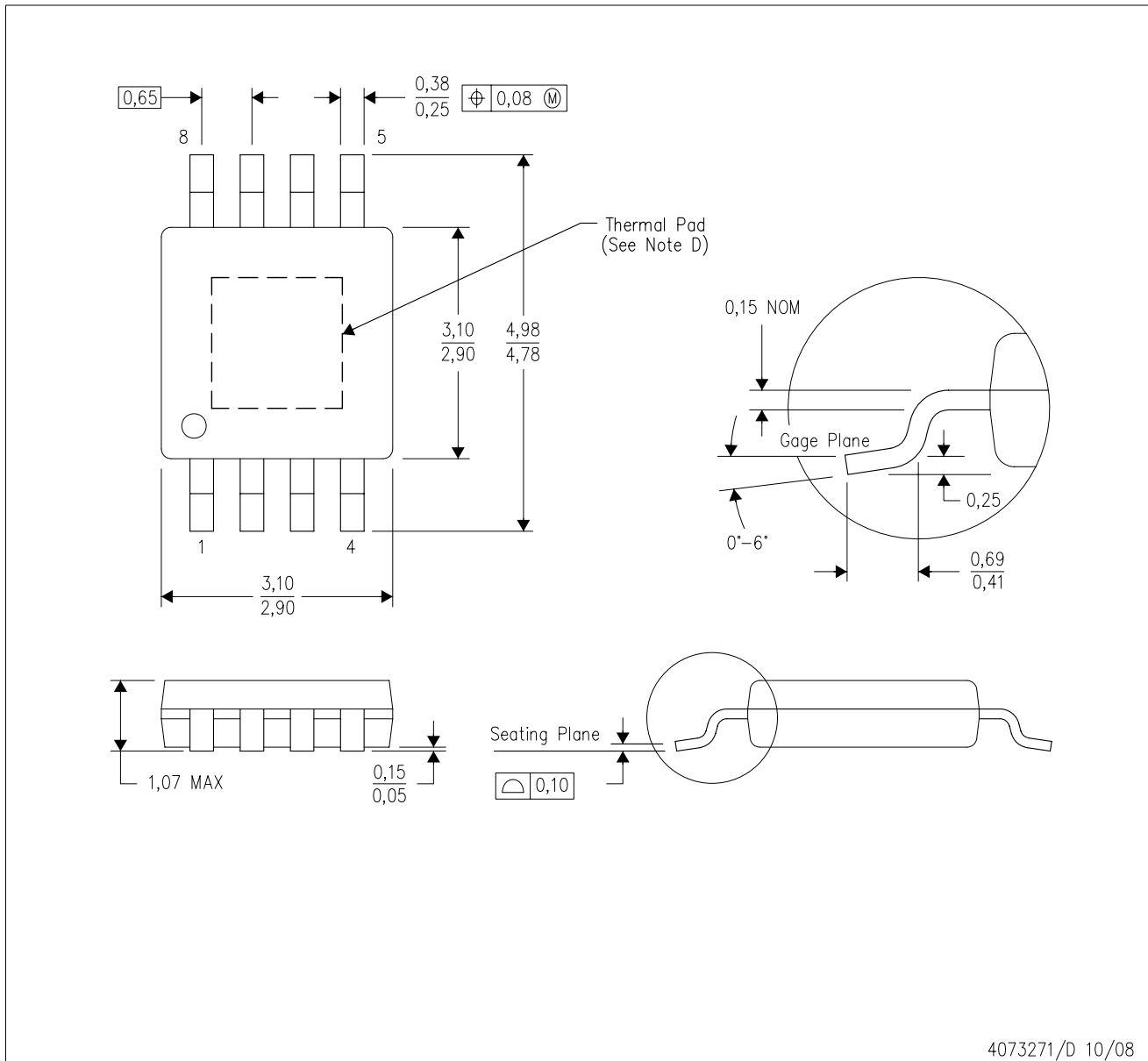
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2060DGNR	MSOP-PowerPAD	DGN	8	2500	370.0	355.0	55.0
TPS2064DGNR	MSOP-PowerPAD	DGN	8	2500	370.0	355.0	55.0
TPS2068DGNR	MSOP-PowerPAD	DGN	8	2500	370.0	355.0	55.0
TPS2068DR	SOIC	D	8	2500	533.4	186.0	36.0
TPS2069DGNR	MSOP-PowerPAD	DGN	8	2500	370.0	355.0	55.0



# MECHANICAL DATA

DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Falls within JEDEC MO-187

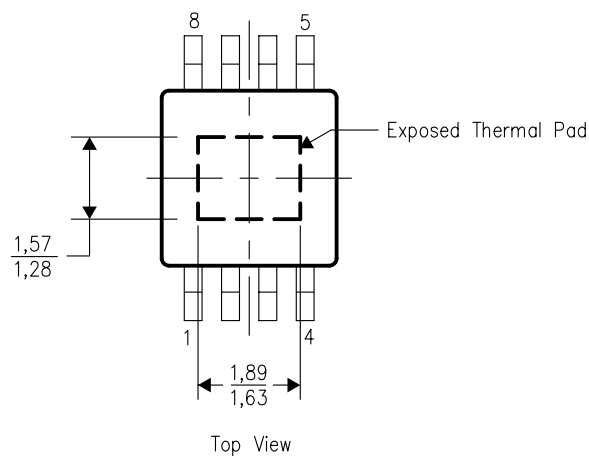
PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

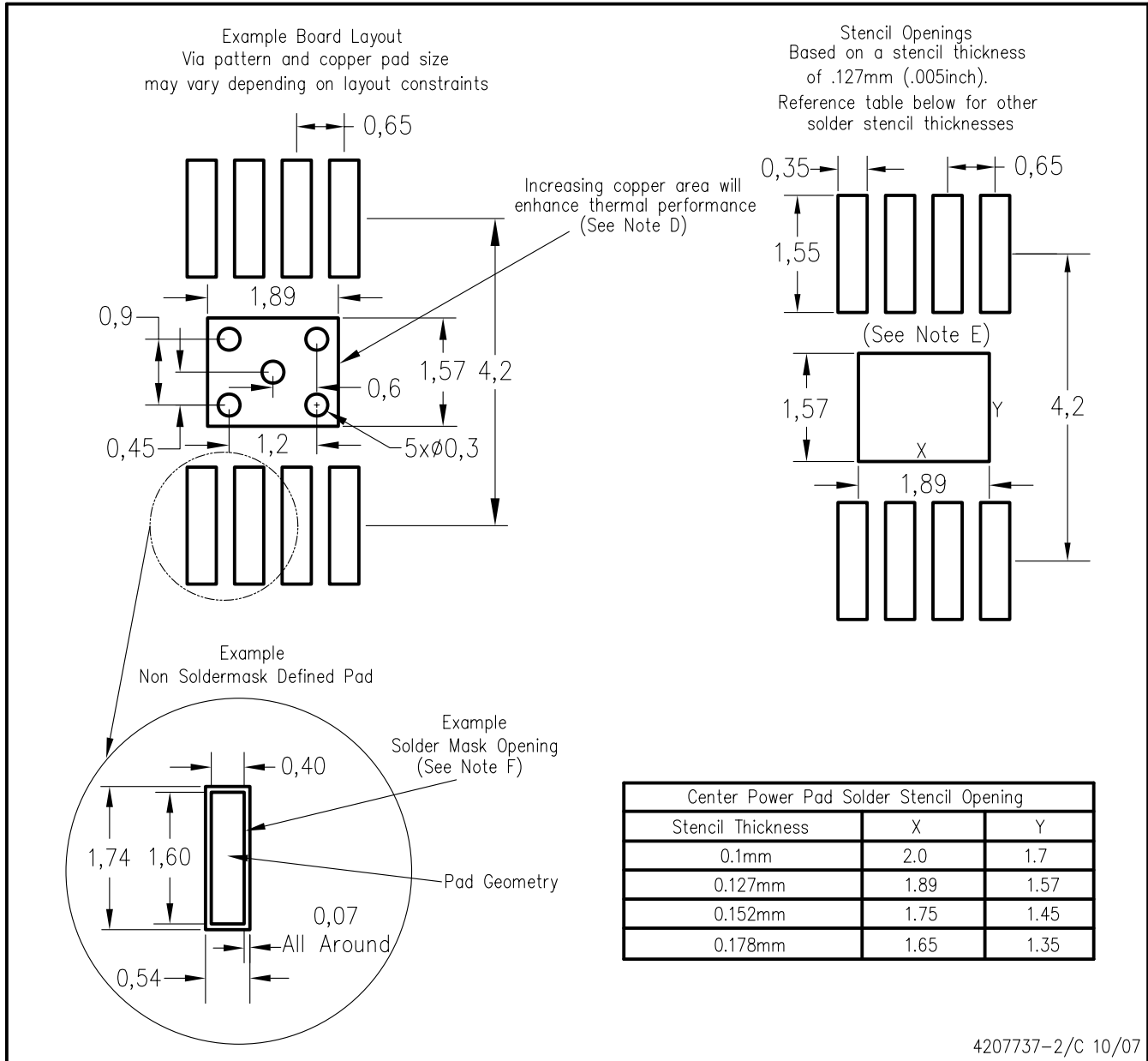
The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DGN (R-PDS0-G8) PowerPAD™

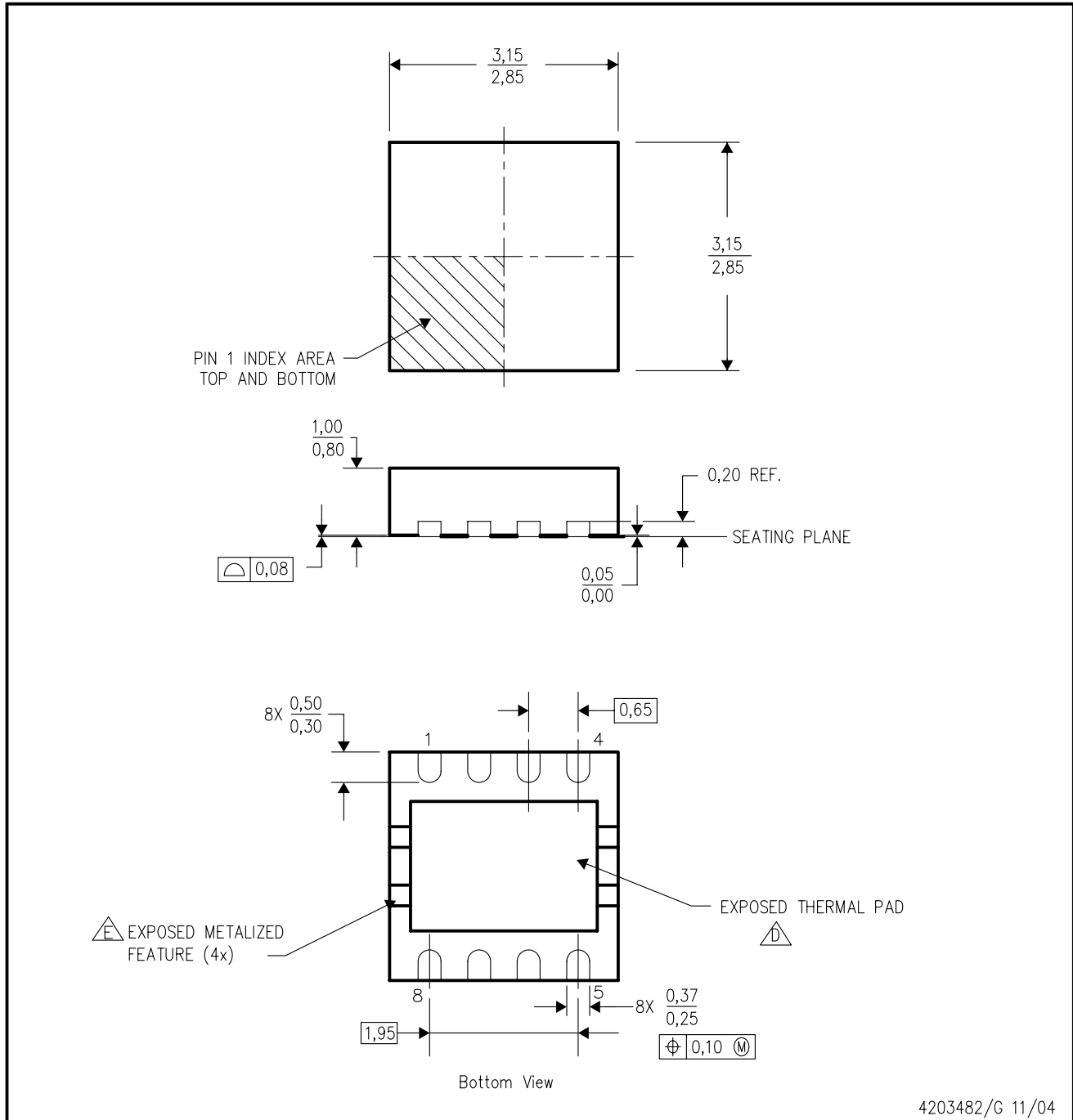


4207737-2/C 10/07

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DRB (S-PDSO-N8)

PLASTIC SMALL OUTLINE



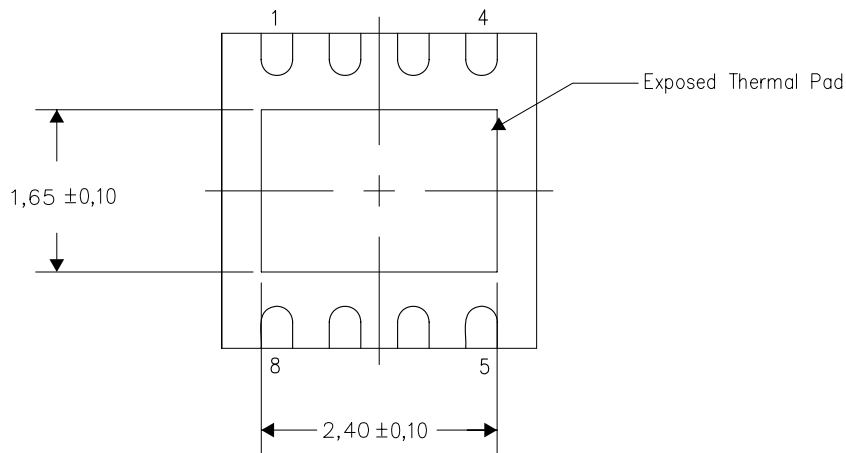
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Small Outline No-Lead (SON) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - Metalized features are supplier options and may not be on the package.

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

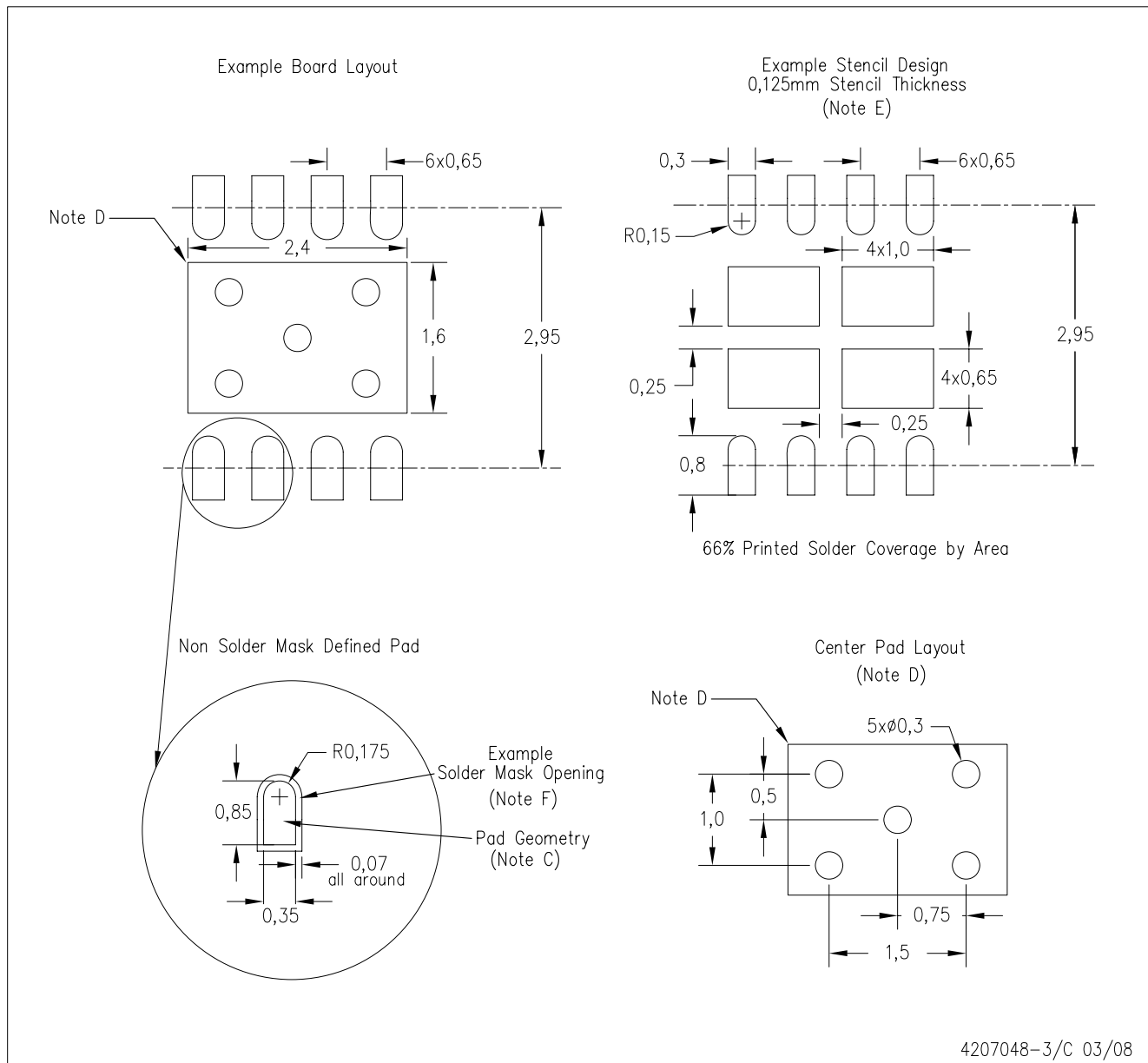


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

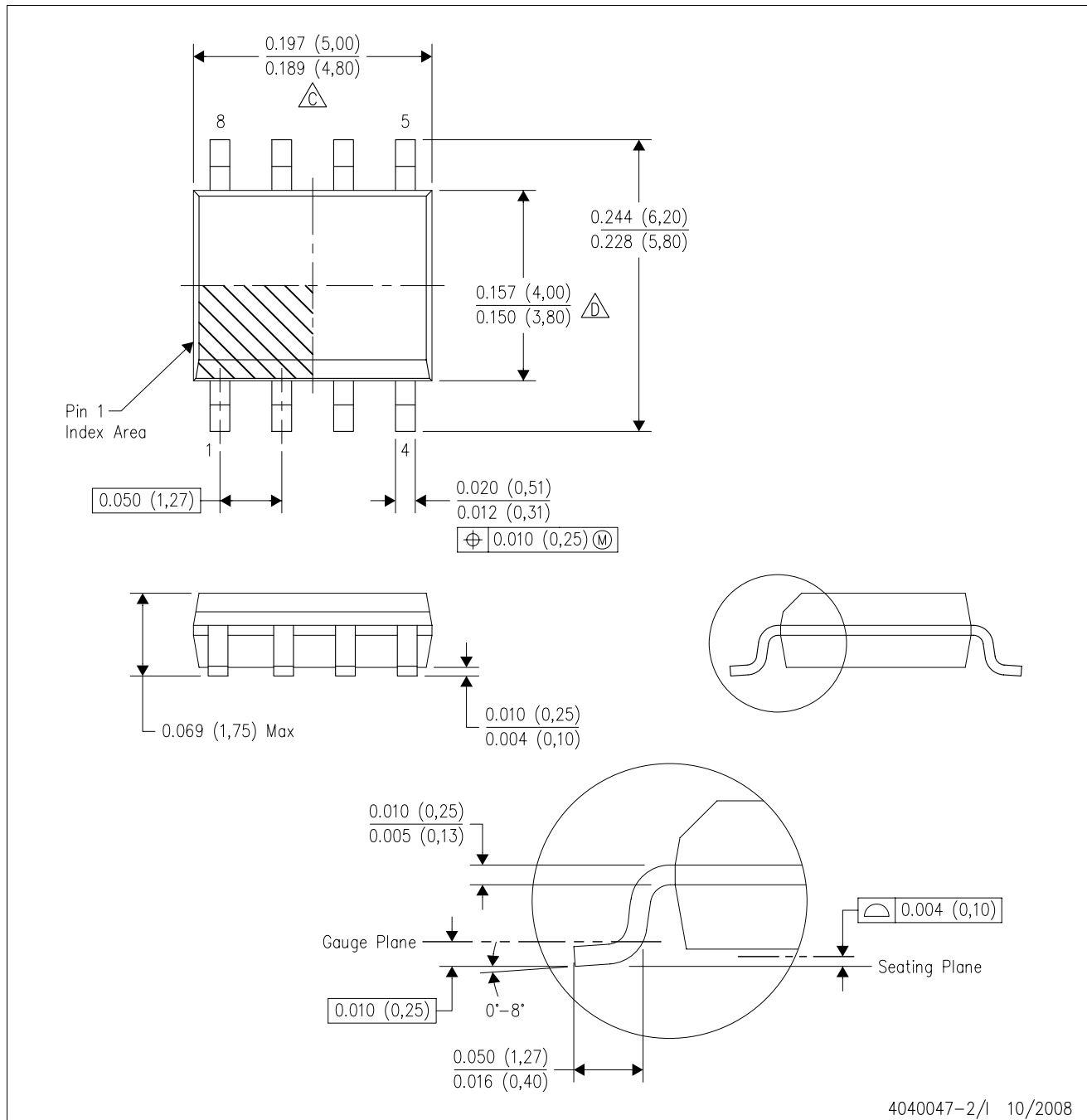
## DRB (S-VSON-N8)



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for solder mask tolerances.

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AA.

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